REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated January 29, 2004 (U.S. Patent Office Paper No. 4). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1 to 11 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1 to 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Barnes, U.S. Patent No. 6,122,315 (further, Barnes '315). Applicants respectfully traverse the rejection.

The present invention as recited in claim 1 is directed to a digital data decompressing system that decompresses compressed digital data to restore original data thereof. The system comprises a plurality of memory areas in which decompressed data is stored; and a plurality of flags each provided to correspond to each of said plurality of memory areas which indicate when all bits of stored data are set to predetermined logical values. When all bits of data to be written to any of the plurality of memory areas are set to predetermined logical values, the corresponding flags are set to a first state.

The present invention as recited in claim 9 is directed to a digital data decompressing method in a digital data decompressing system that comprises a plurality of memory areas in which decompressed data is stored, a plurality of flags each provided to correspond to each of said plurality of memory areas which indicate when all bits of stored data are set to logical "0"s, and an arithmetic circuit for performing computations between data items stored in the plurality of memory areas, the method comprising the steps of inputting digital data compressed in compliance with a predetermined method as a bit stream of a proper format

and performing the restoration of original data by decompressing the bit stream data, and when two data items stored in the memory areas are added and the flag corresponding to one of the two data items to be added is set to a first state, reading data of another memory area whose flag is not set to the first state, storing the data of another memory area in a third memory area in which data after computations is to be stored, and setting the flag corresponding to the memory area to the second state.

The present invention as recited in claim 10 is directed to a digital data decompressing method in a digital data decompressing system that comprises a plurality of memory areas in which decompressed data is stored, a plurality of flags, each provided ~~so as~~ to correspond to each of said plurality of memory areas which indicate when all bits of stored data are set to logical "0"s, and an arithmetic circuit for performing computations between data items stored in the plurality of memory areas, the method comprising the steps of inputting digital data compressed in compliance with a predetermined method as a bit stream of a proper format and performing the restoration of original data by decompressing the bit stream data, and when two data items stored in the memory areas are multiplied and the flag corresponding to one of the two data items to be multiplied is set to a first state, setting the flag corresponding to a third memory area in which data after multiplication is to be stored to the first state.

The present invention as recited in claim 11 is directed to A digital data decompressing method in a digital data decompressing system that comprises a plurality of memory areas in which decompressed data is stored, and a plurality of flags provided to correspond to each of said plurality of memory areas, which indicate when all bits of stored data logical "0"s, the method comprising the steps of inputting digital data compressed in compliance with a predetermined method as a bit stream of a proper format and performing the restoration of original data by decompressing the bit stream data, whereas performing counting of the number of valid data, storing successively the valid data to be decompressed in the plural memory areas and setting the flags corresponding to the memory areas to the first state, and when the valid data is exhausted, setting the flags corresponding to remaining memory areas in which data to be decoded is to be stored to a second state.

Among the main features of the present invention, each of the a plurality of flags indicates whether every bit of stored data has a predetermined logical value, for example “0”. By referring to each flag, a control circuit can avoid performing a wasteful writing/reading

process, and implicitly the power consumption can be reduced and the computation time can be shortened.

With respect to Barnes '315, the Examiner alleged in the Office Action mailed on August 13, 2003 (Paper No. 2), on page 2 that Figs. 6 and 9c, the Abstract, col. 10, lines 30+, and col. 11, lines 1+, of Barnes '315 all show a digital decompression system that renders obvious the digital data decompressing system of claim 1. However, the Examiner conceded, on the same page 2 of that Office Action that Barnes '315 fails to explicitly teach predetermined logical value. The Examiner found that, because Barnes '315 teaches the logical values, plurality of memory areas, status flag and four states of the logical values, it was obvious that the four states of logical values are preset or predetermined logical values.

The Examiner then alleged in the Office Action mailed on January 29, 2004 (Paper No. 5) that the arguments submitted by Applicants in response to the rejection formulated in the Office Action (Paper No. 2) have no merit and the rejection still applies. The position of the Examiner as to Barnes '315 disclosing all features of the invention and as rendering obvious the present invention, as claimed in claim 1, is respectfully traversed.

Applicants will submit that Barnes '315 merely discloses a flag for indicating whether FIFOs are empty or full. The decoder apparatus disclosed by Barnes '315 does not write data to a FIFO if the status flag indicates full and does not read data from the FIFO if the status flag indicates empty. Applicants further submit that the status flag of Barnes '315 merely provides information whether data can be written to a FIFO or if data can be read from a FIFO. Therefore, the disclosure of Barnes '315 does not disclose, teach or suggest a plurality of flags, each provided to correspond to each of said plurality of memory areas, which indicate when all bits of stored data are set to predetermined logical values, wherein, when all bits of data to be written to any of the plurality of memory areas are set to predetermined logical values, the corresponding flags are set to a first state, as recited in at least claim 1.

In view of the foregoing, Applicants will respectfully contend that claim 1 and dependent claims 2 to 8 are not rendered obvious under 35 U.S.C. §103(a) by Barnes '315. Withdrawal of the 35 U.S.C. §103 (a) rejection of claims 1 to 8 is respectfully requested.

The Examiner alleged in the Office Action mailed August 13, 2003 (Paper No. 2) on page 3 thereof, regarding claims 9 to 11, that the claimed limitations of claims 9 to 11 are

substantially similar to the ones of claims 1 to 4 therefore the grounds for rejecting claims 1 to 4 also apply to those claims.

Applicants will submit that the arguments presented above outlining how the teachings of Barnes '315 do not render obvious the recitation of claims 1 to 8 also apply in distinguishing the invention as recited in claims 9 to 11 from Barnes '315. Consequently, the invention recited in claims 9 to 11 is also distinguishable and thereby allowable over the prior art.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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